Ordering number: 2134B

Thick Film Hybrid IC

STK4040V

AF Power Amplifier (Split Power Supply) (70W min, THD = 0.08%)

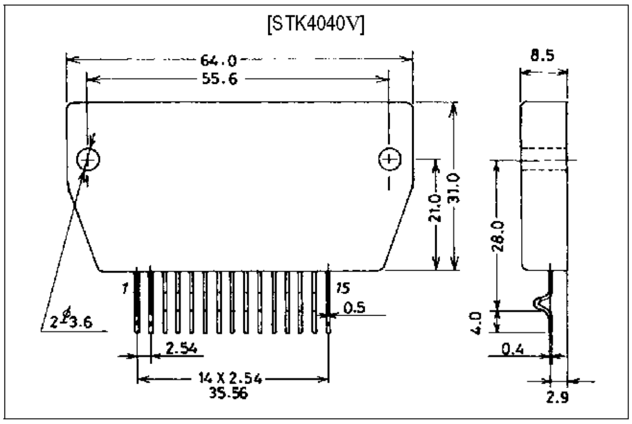
Features

- Small-sized package permitting audio sets to be made slimmer (up to 70W)
- The STK4024Vseries are available for output 20W to 100W (200W) and are pin-compatible. (120W to 200W : 18 pins)
- Facilitates thermal design of slim stereo sets.
- Distortion 0.08% due to current mirror circuit
- Possible to design electronic supplementary circuits (pop noise muting at the time of power ON/OFF, load short protector, thermal shutdown)

Package Dimensions

unit: mm

4062



Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		±62	V
Thermal resistance	θj-c		1.4	°C/W
Junction Temperature	Tj		150	°C
Operating substrate temperature	Tc		125	°C
Storage temperature	Tstg		–30 to +125	°C
Available time for load short-circuit	t_s*1	V_{CC} = ±42V, R_L = 8Ω, f = 50Hz, Po = 70W	1	s

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		±42	V
Load resistance	R_L		8	Ω

SANYO Electric Co., Ltd. Semiconductor Business Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

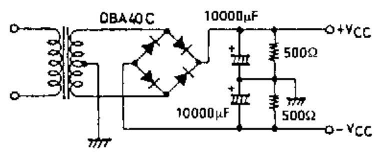
Operating Characteristics at Ta = 25°C, V_{CC} = ±42V, R_L = 8Ω, VG = 40dB, Rg = 600Ω, 100kHz LPF ON, R_L : noninductive load

Parameter	Symbol	Conditions	min	typ	max	Unit
Quiescent current	Icco	V_{CC} = ±50.5V	15		120	mA
Output power	Po (1)	THD = 0.08%, f = 20Hz to 20kHz	70			W
	Po (2)	V_{CC} = ±36V, THD = 0.2%, R_L = 4Ω, f = 1kHz	70			W
Total harmonic distortion	THD	Po = 1.0W, f = 1kHz			0.08	%
Frequency response	f_L, f_H	Po = 1.0W, $^{+0}_{-3}$ dB		20 to 50k		Hz
Input impedance	r_i	Po = 1.0W, f = 1kHz		55		kΩ
Output noise voltage	V_{NO} *2	V_{CC} = ±50.5V, Rg = 10kΩ			1.2	mVrms
Neutral voltage	V_N	V_{CC} = ±50.5V	–70	0	+70	mV

Notes. For power supply at the time of test, use a constant-voltage power supply unless otherwise specified.

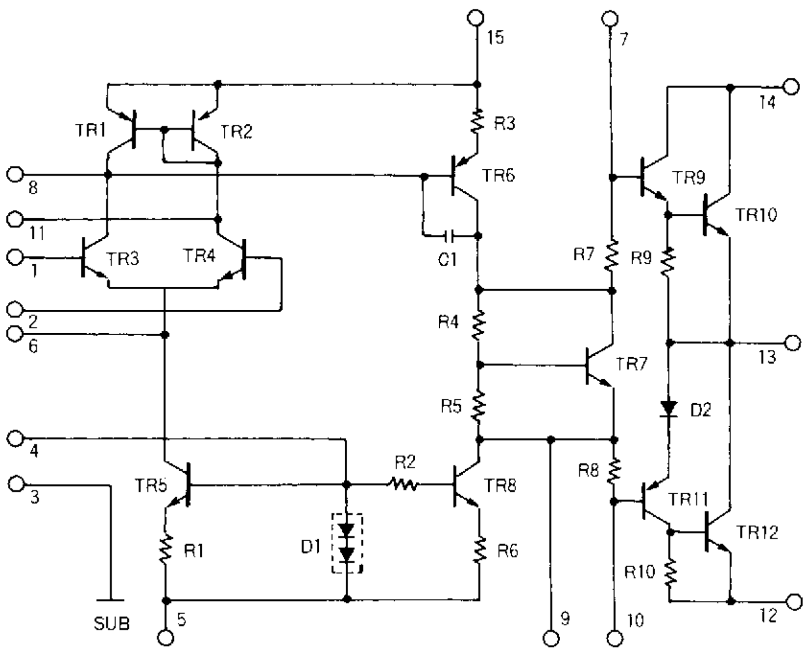
*1 For measurement of the available time for load short-circuit and output noise voltage, use the specified transformer power supply shown right.

*2 The output noise voltage is represented by the peak value on rms scale (VTVM) of average value indicating type. The noise voltage waveform includes no flicker noise.

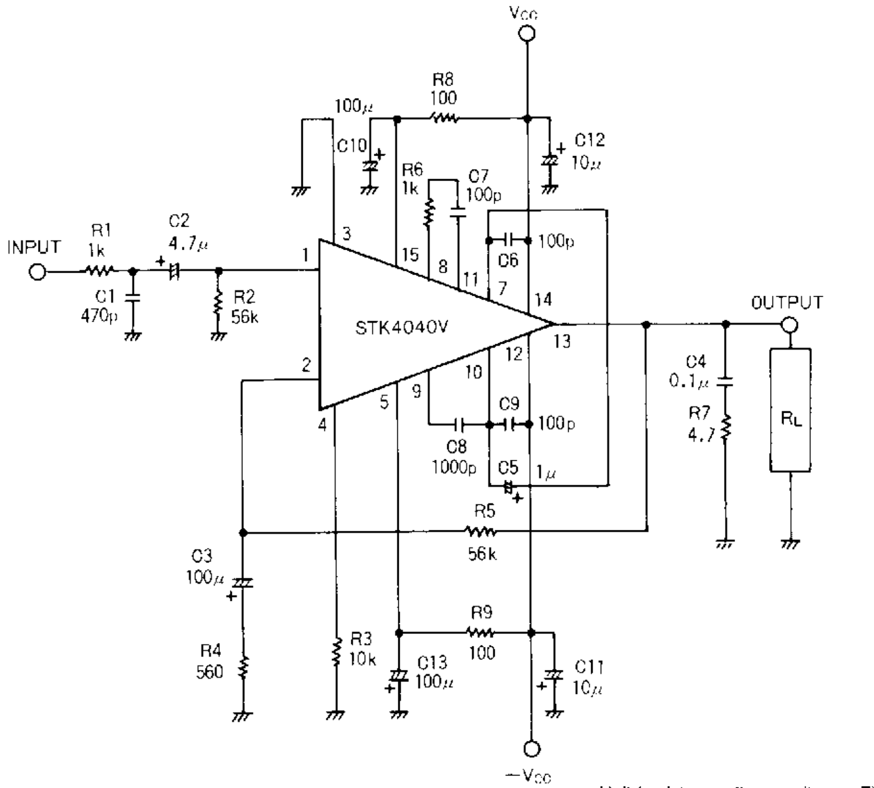


Specified Transformer Power Supply
(Equivalent to MG-200)

Equivalent Circuit

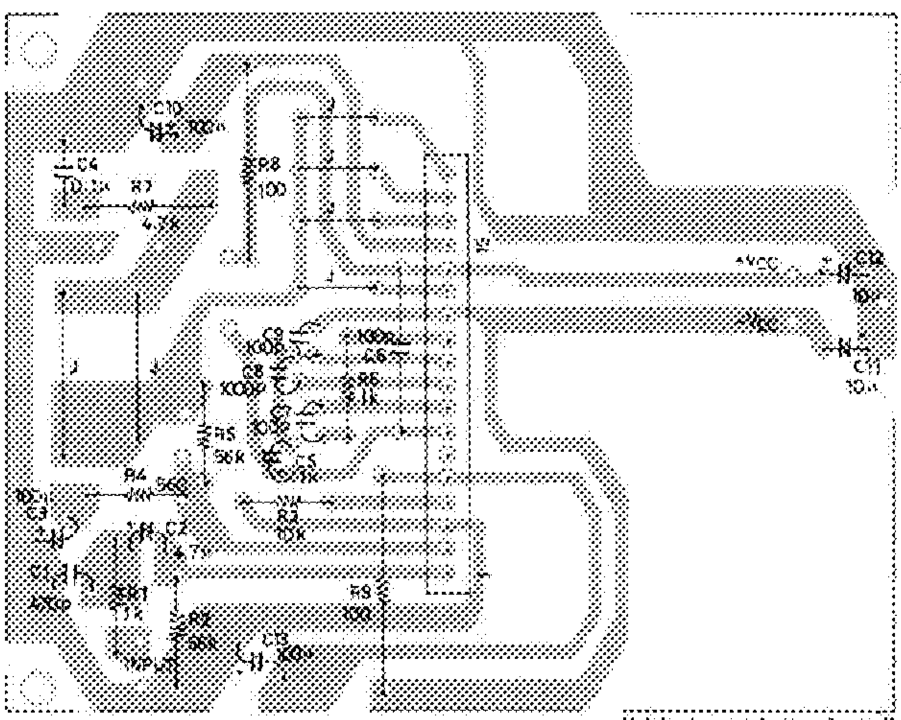


Sample Application Circuit: 70W min Single-Channel AF Power Amplifier

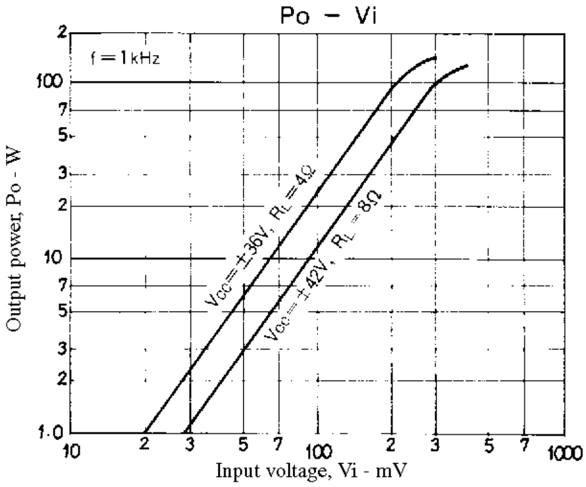


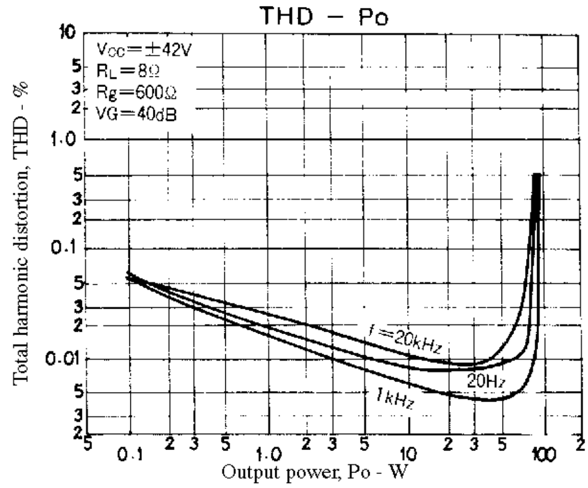
Unit (resistance: Ω, capacitance: F)

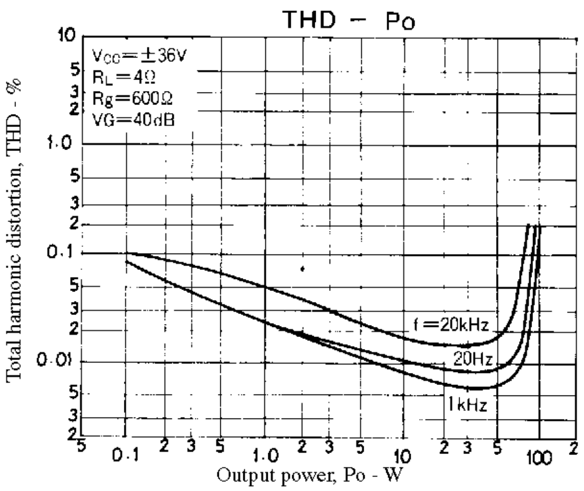
Sample Printed Circuit Pattern for Application Circuit (Cu-foiled side)

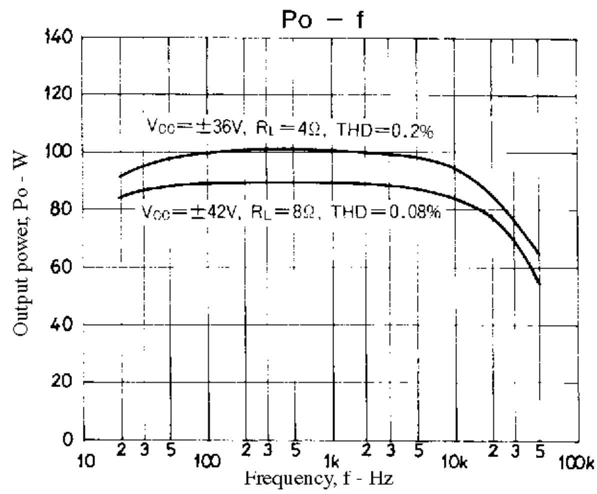


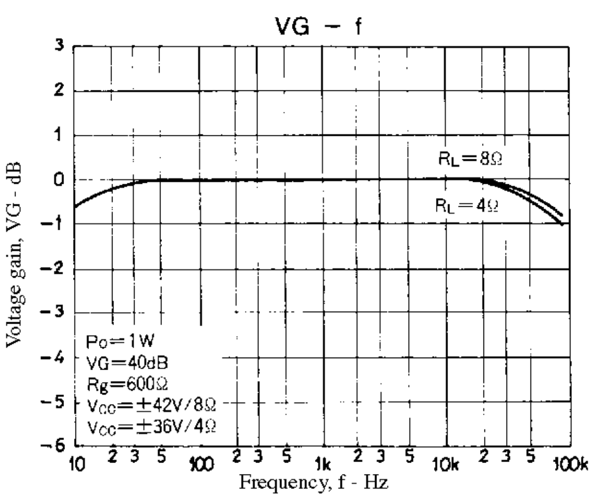
Unit (resistance: Ω, capacitance: F)

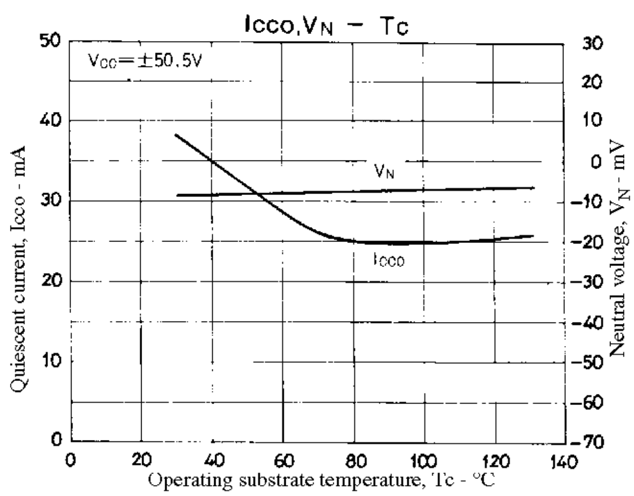

Po – Vi
f = 1kHz
V_{CC}=±36V, R_L=4Ω
V_{CC}=±42V, R_L=8Ω
Output power, Po - W
Input voltage, Vi - mV

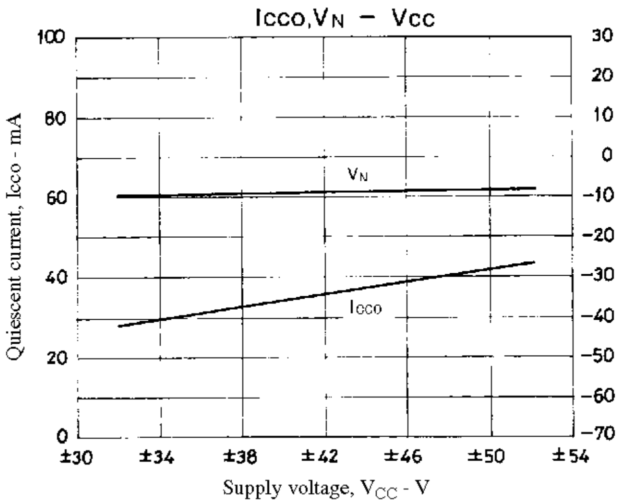

THD – Po
V_{CC}=±42V
R_L=8Ω
Rg=600Ω
VG=40dB
f=20kHz
20Hz
1kHz
Total harmonic distortion, THD - %
Output power, Po - W

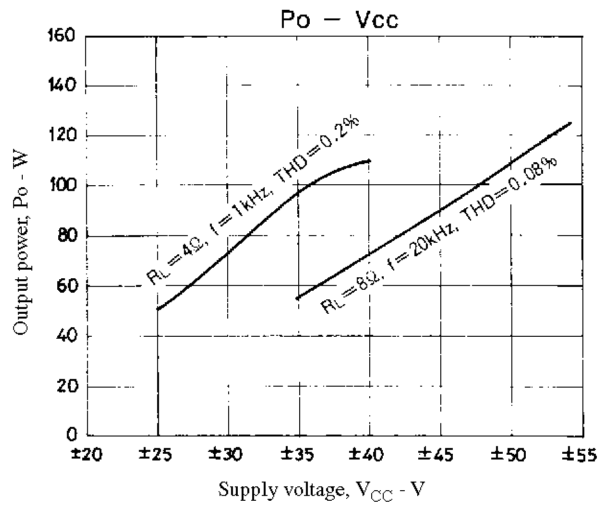

THD – Po
V_{CC}=±36V
R_L=4Ω
Rg=600Ω
VG=40dB
f=20kHz
20Hz
1kHz
Total harmonic distortion, THD - %
Output power, Po - W

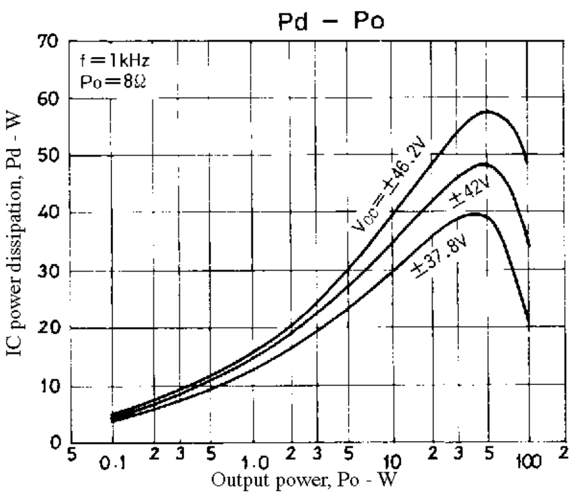

Po – f
V_{CC}=±36V, R_L=4Ω, THD=0.2%
V_{CC}=±42V, R_L=8Ω, THD=0.08%
Output power, Po - W
Frequency, f - Hz

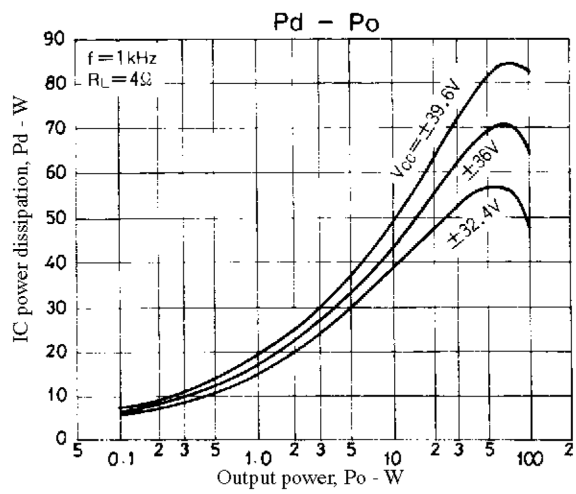

VG – f
R_L=8Ω
R_L=4Ω
Po=1W
VG=40dB
Rg=600Ω
V_{CC}=±42V/8Ω
V_{CC}=±36V/4Ω
Voltage gain, VG - dB
Frequency, f - Hz

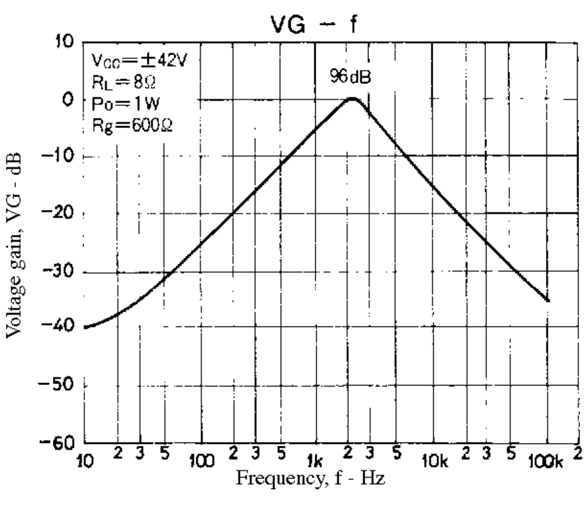

Icco, V_N – Tc
V_{CC}=±50.5V
V_N
Icco
Quiescent current, Icco - mA
Neutral voltage, V_N - mV
Operating substrate temperature, Tc - °C

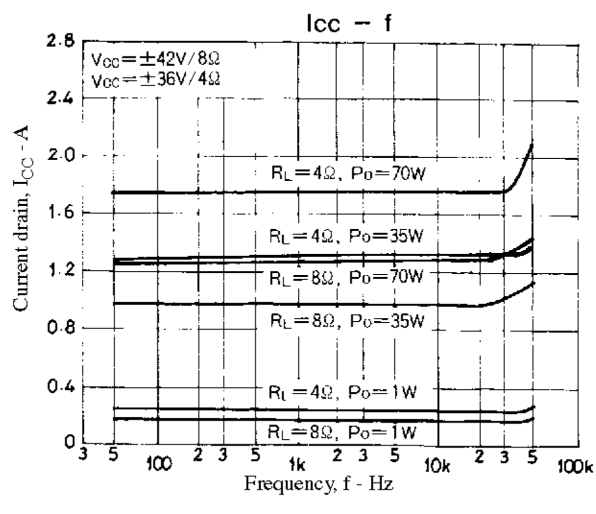

Icco,VN – Vcc
VN
Icco
Quiescent current, Icco - mA
Neutral voltage, VN - mV
Supply voltage, VCC - V
100
80
60
40
20
0
30
20
10
0
–10
–20
–30
–40
–50
–60
–70
±30
±34
±38
±42
±46
±50
±54

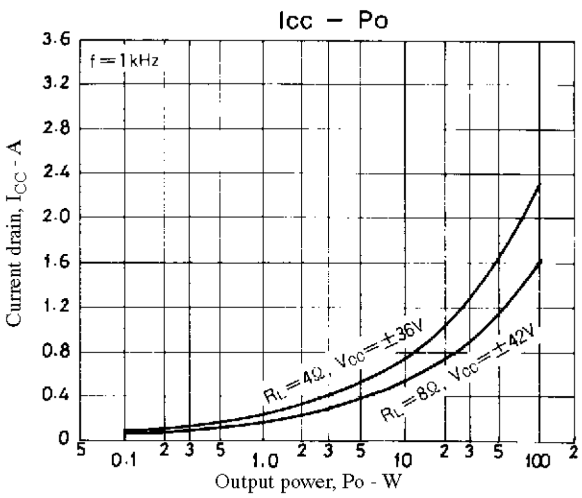

Po – Vcc
RL=4Ω, f=1kHz, THD=0.2%
RL=8Ω, f=20kHz, THD=0.08%
Output power, Po - W
Supply voltage, VCC - V
160
140
120
100
80
60
40
20
0
±20
±25
±30
±35
±40
±45
±50
±55

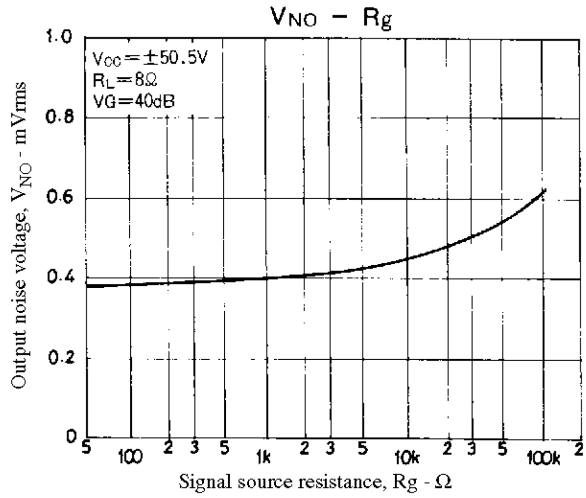

Pd – Po
f=1kHz
Po=8Ω
VCC=±46.2V
±42V
±37.8V
IC power dissipation, Pd - W
Output power, Po - W
70
60
50
40
30
20
10
0
5
0.1
2
3
5
1.0
2
3
5
10
2
3
5
100
2


Pd – Po
f=1kHz
RL=4Ω
VCC=±39.6V
±36V
±32.4V
IC power dissipation, Pd - W
Output power, Po - W
90
80
70
60
50
40
30
20
10
0
5
0.1
2
3
5
1.0
2
3
5
10
2
3
5
100
2

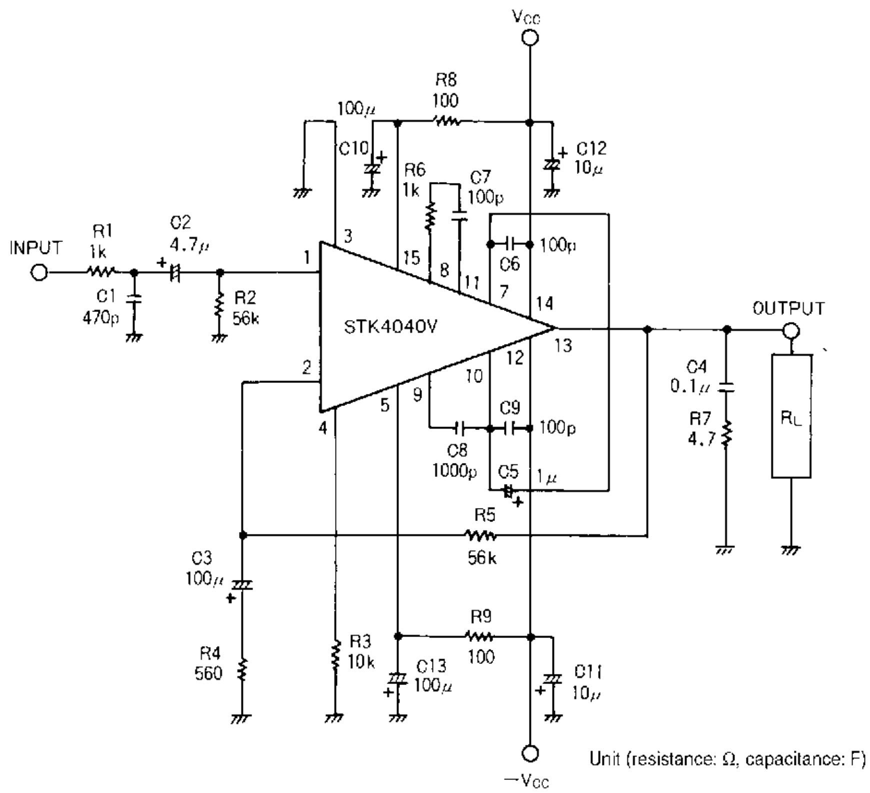

VG – f
VCC=±42V
RL=8Ω
Po=1W
Rg=600Ω
96dB
Voltage gain, VG - dB
Frequency, f - Hz
10
0
–10
–20
–30
–40
–50
–60
10
2
3
5
100
2
3
5
1k
2
3
5
10k
2
3
5
100k
2

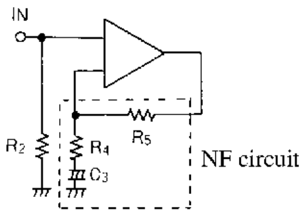

Icc – f
VCC=±42V/8Ω
VCC=±36V/4Ω
RL=4Ω, Po=70W
RL=4Ω, Po=35W
RL=8Ω, Po=70W
RL=8Ω, Po=35W
RL=4Ω, Po=1W
RL=8Ω, Po=1W
Current drain, ICC - A
Frequency, f - Hz
2.8
2.4
2.0
1.6
1.2
0.8
0.4
0
3
5
100
2
3
5
1k
2
3
5
10k
2
3
5
100k



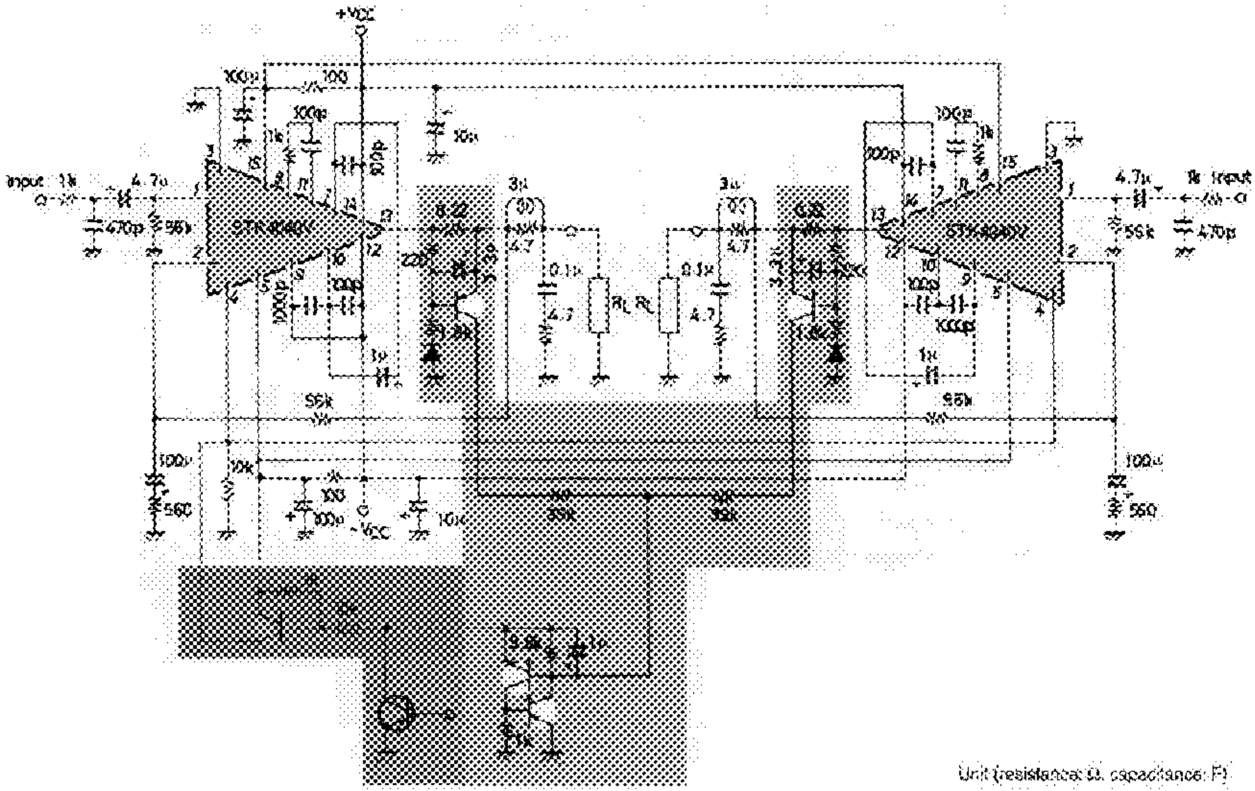


Description of External Parts



R1, C1	Input filter circuit • Used to reduce noise at high frequencies.
C2	Input coupling capacitor • Used to block DC current. When the reactance of the capacitor increases at low frequencies, the dependence of 1/f noise on signal source resistance causes the output noise to worsen. It is better to decrease the reactance.
R2	Input bias resistor • Used to bias the input pin to zero. • Affects V_N stability. (See NF circuit.) • Because of differential input, this resistor fixes the input resistance practically.
R4, R5 C3 (R2)	NFB circuit (AC NF circuit). It is desirable that the error of the resistor value is 1% or less.  C3 : Capacitor for AC NF R4, R5 : Used to set VG • VG setting obtained by using R4, R5 $\log 20 \cdot \frac{R_5}{R_4}$ 40dB is recommended. • Low cutoff frequency setting obtained by using, R4, C3. $f_L = \frac{1}{2\pi \cdot R_4 \cdot C_3} [Hz]$ To change VG setting, it is desirable to change R4. In this case, the low cutoff frequency setting needs to be rechecked. When VG setting is changed by changing R5, R5 must be made equal to R2 to ensure V_N balance. If the resistor value is increased more than the existing value, it may be hard to ensure V_N balance and the temperature characteristic of V_N may be also deteriorated.
R3	Differential constant-current bias resistor
R6, R7	Used for oscillation blocking and phase compensation
R7, C4	Used for oscillation blocking and phase compensation (C4 : A polyester film capacitor is recommended.)
C6, C9	Used for oscillation blocking and phase compensation Power amp stage (Must be connected near the pin) C6 : Power amp on (+) side C9 : Power amp on (–) side
C8	Used for oscillation blocking and phase compensation (Used for oscillation blocking before clip at power amp stage)
C5	Used for oscillation blocking and distortion improvement
R8, C10	Ripple filter circuit on (+) side
R9, C13	Ripple filter circuit on (–) side
C11, C12	Used for oscillation blocking • Used to decrease the power supply impedance to operate the IC stably. Must be connected near the IC pin. It is desirable to use an electrolytic capacitor.

Sample Application Circuit (protection circuit and muting circuit)



Thermal Design

The IC power dissipation of the STK4040V at the IC-operated mode is 47.4W max. at load resistance 8Ω and 70.5W max. at load resistance 4Ω for continuous sine wave as shown in Figure 1 and 2.

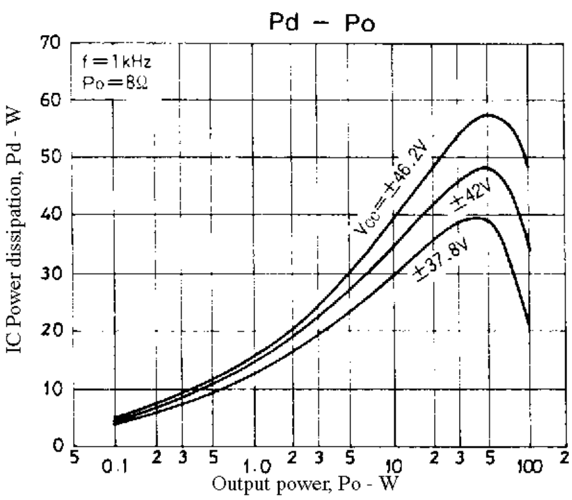


Figure 1. STK4040V Pd – Po (R_L = 8Ω)

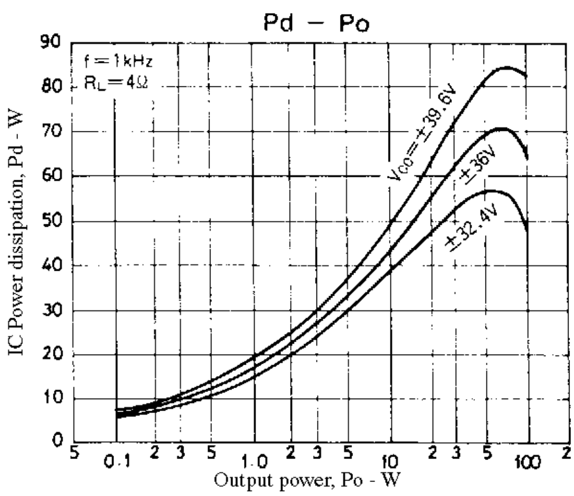


Figure 2. STK4040V Pd – Po (R_L = 4Ω)

In an actual application where a music signal is used, it is impractical to estimate the power dissipation based on the continuous signal as shown above, because too large a heat sink must be used. It is reasonable to estimate the power dissipation as 1/10 Po max. (EIAJ).

That is, Pd = 30.6W at 8Ω, Pd = 38.2W at 4Ω

Thermal resistance θc-a of a heat sink for this IC power dissipation (Pd) is fixed under conditions 1 and 2 shown below.

Condition 1: $T_C = Pd \times \theta c\text{-}a + Ta \leq 125°C$ .... (1)

where Ta : Specified ambient temperature

T_C : Operating substrate temperature

Condition 2: $Tj = Pd \times (\theta c\text{-}a) + Pd/2 \times (\theta j\text{-}c) + Ta \leq 150°C$..................... (2)

where Tj : Junction temperature of power transistor

Assuming that the power dissipation is shared equally between the two power transistors, thermal resistance θj-c is 1.4°C/W and

$$Pd \times (\theta c\text{-}a + 1.4/2) + Ta \leq 150°C \quad (3)$$

Thermal resistance θc-a of a heat sink must satisfy inequalities (1) and (3).

Figure 3 shows the relation between Pd and θc-a given from (1) and (3) with Ta as a parameter.

[Example] The thermal resistance of a heat sink is obtained when the ambient temperature specified for a stereo amplifier is 50°C.

Assuming $V_{CC} = \pm 42V$, $R_L = 8\Omega$,

$V_{CC} = \pm 36V$, $R_L = 4\Omega$,

$R_L = 8\Omega$: Pd1 = 30.6W at 1/10 Po max.

$R_L = 4\Omega$: Pd2 = 38.2W at 1/10 Po max.

The thermal resistance of a heat sink is obtained from Figure 3.

$R_L = 8\Omega$: θc-a1 = 2.45°C/W

$R_L = 4\Omega$: θc-a2 = 1.89°C/W

Tj when a heat sink is used is obtained from (3).

$R_L = 8\Omega$: Tj = 146.4°C

$R_L = 4\Omega$: Tj = 148.9°C

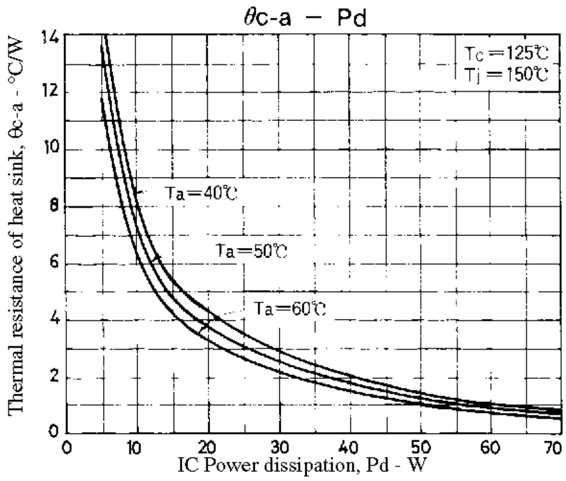


Figure 3. STK4040V θc-a – Pd

This design is based on the use of a constant-voltage regulated power supply. Pd differs when a transformer power supply is used. Redesign must be made based on Pd that suits the regulation of each transformer.

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